REMARKS

Section 101 Rejection of Claims 1-25

Referring to M.P.E.P. § 2106, the required analysis involves the determination of whether there is a practical application of an abstract idea and whether the claimed solution preempts a judicial exception. See page 2100-11.

That is not the case here. Specifically, in each of the claims, there is a practical application of an abstract idea because the claim produces a useful concrete and tangible result. There is not a preempting of a judicial exceptions because each of the claims is limited in its wording to a specific application, namely, that of a response compactor.

Therefore, reconsideration is requested.

Claim 1 calls for a method of developing "a response compactor." Thus, the claim cannot possibly preempt a judicial exception. It is clearly useful since response compactors are useful. It is clearly concrete because it is repeatable. See M.P.E.P. § 2106 at page 2100-12. It is clearly a tangible result since the result of a method is to develop something that has a practical application; that is, a response compactor.

Claim 9 calls for a response compactor and, for the reasons described above, satisfies the requirements of Section 101. Likewise, claim 16 calls for a response compactor and, for the reasons described above, satisfies the requirements of Section 101.

Section 112 Rejections

The office action poses a number of rejections under Section 112. While some of these rejections appear to be more questions than rejections, each of the questions or rejections will be addressed individually in the following discussion.

1. In Claim 1, what is meant by "adding at least two columns to a compactor matrix for each circuit output that, at the same time, produced an unknown logic value?

To the extent there is an objection under Section 112, it is submitted that there is nothing unclear about any of the words as amended. Each of the words used simple words that would be well known to one skilled in the art. The claim has been amended to clarify that when two scan

chains produce unknown logic values at the same time, columns are added to the compactor matrix.

To the extent some clarification is requested, the following comments can be provided. As explained at page 5, lines 1-8, for every combination of K scan chains, K+1 columns are added to the compactor matrix, in one embodiment. The value K is the number of unknown logic values produced at the same time. See the specification at page 4, lines 18-20. Thus, the specification at page 5, lines 2-8 give a simple example. If there are a hundred scan chains and K=2, 100x99x98÷6 (3x2x1) where almost 160 combinations are possible. An example where K=2, K+1=3 and there are almost 480,000 columns that result from taking every combination of scan ins in groups of three. Thus, the idea is that for every unknown value that occurs at the same time on two scan chains, you add two columns to the compactor matrix. A compactor matrix it is shown, for example, in Figure 3.

Therefore, reconsideration is requested.

2. What is the result of adding? What is it for?

See above. The result of adding is that you can handle any number of unknown logic values that occur at the same time.

3. What it is related to the unknown logic value?

The unknown logic value is explained on page 3 of the specification at lines 21-25. Some scan chains can produce logic values unknown during stimulation at the same scan on cycle when some other scan chains produce an error. In that case, there is a chance that this error can get masked and the defect is not detected.

4. As per claim 2, lines 1-2, "adding at least two columns ... at the same time" is not clear as to what it meant.
How is it related to the unknown logic values?
In addition, line 2 "can" a positive term should be used.

The claim is canceled.

5. As per claim 3, this claim is also rejected
because it is dependent upon the rejected base claim.

Reconsideration is requested in view of the comments and amendments above.

6. As per claim 4, lines 1-3, "wherein adding at least one column ... unknown logic value includes adding two columns ... for each scan chain" the claim is not clear because the word "wherein" is referred to any step or means that is mentioned before and "includes adding two columns to the matrix for each such scan chain," this limitation already cited in claim 2.

Claim 4 has been canceled.

7. As per claim 5, lines 1-2, "reducing the compactor matrix using maximum class problem" what is meant by using maximum compatibility class problem?

It is respectfully submitted that the maximum compatibility class problem is known to one skilled in the art. See The Architecture of Pipelined Computers, by Peter M. Kogge, 1981, at page 98 ("A compatibility class with respect to Hc mod p is a subset of Zp in which all pairs of elements are compatible." "A maximum compatibility class with respect to Hc mod p is a compatibility class that is not a subset of any other compatibility class").

8. As per claim 6, this claim is also rejected
because it is dependent upon the rejected base claim.

Reconsideration is requested.

9. As per claim 7, line 1, "a compactor maxtrix"
should be changed to --the compactor matrix--.

This change has been made.

10. As per claim 8, this claim is also rejected
because it is dependent upon the rejected base claim.

Reconsideration is requested.

11. As per claim 9, lines 5-6, "adding at least two columns ... produce unknown logic value" it is not clear what is the result of adding and what is it for? How is it related to unknown logic values?

It is believed that this is addressed in item number 1 above.

12. As per claim 10, line 1, "a process" and "a number"
should be changed to --the process-- and --the number--;
in line 2, "can" a positive term should be used.

These changes have been made.

13. As per claim 11, line 1, "a process" should be changed to --the process--.

The change has been made.

14. Lines 2-4, wherein adding at least one column ... unknown logic values includes adding two columns -- for each scan chain." The claim is not clear because the word "wherein" is referred to and step or mean that is mentioned before and includes adding two columns to the matrix for each said scan chain, this limitation is already recited in claim 9.

The claim has already been canceled.

15. As per claim 12, this claim is also rejected
because it is dependent upon the rejected base claim.

Reconsideration is requested.

16. As per claim 13, line 1, "a process" should be changed to --the process--.

The change has been made.

17. As per claim 14, line 1 "a process" should be changed to --the process--.

The change has been made.

18. Line 2, "a compactor matrix" should be changed to --the compactor matrix-- and line 3 "can" a positive term should be used.

The changes have been made and the word "can" has been eliminated.

19. As per claim 15, line 1, "a process" should be changed to --the process--.

The change has been made.

20. As per claim 16, lines 1-3, "a response compactor ... to handle any number of scan chains with unknown logic values" the claim as a whole is not understood. It is unclear how the exclusive OR gates are coupled (parallel or series)? And how they handle any number of scan chains with unknown values?

It is respectfully submitted that it is not the function of the claims to tell how to implement the invention. That is the function of the specification. The claims are general enough that gates may be coupled in any way, series, or parallel. The coupling of the gates is taught in the specification. How they could handle any number of scan changes unknown logic values is described in the specification. By adding two chains, enough information is provided to overcome the problem of the chain with unknown values.

21. As per claim 17, lines 1-2, "to handle any number of errors in the scan chain," it is not clear how they handle any number of errors in the same scan cycle.

The simple answer is that they do and the fact that this is not obvious does not give rise to an objection to the claim.

22. As per claim 18, this claim is also rejected because it is dependent upon the rejected base claim.

Reconsideration is requested.

23. As per claim 19, lines 3-4, "add at least two columns to a compactor matrix: ... produce an unknown logic value," what is meant by "add at least two columns to a compactor matrix for each circuit output that, as the same time produce an unknown logic value? What is the result of adding, what is it for, and how is it related to the unknown logic value?

Please see the responses to questions 1-3 above.

24. As per claim 20, line 2, "a processor-based system" should be changed to --the processor-based system--.

The change has been made.

25. Line 2, "can" a positive term should be used.

The change has been made.

26. As per claim 21, lines 1-2, "a processor-based system" should be changed to --the processor-based system--.

The change has been made.

27. As per claim 22, lines 1-2, "storing instructions that, if executed, enable the compactor matrix to be reduced using maximum capability class problem" is not clear as to what is meant.

It is believed that this issue is responded to in number 7 above.

28. As per claim 23, lines 1-2, "a processor-based system" should be changed to --the processor-based system.

The change has been made.

29. As per claims 24 and 25, "a processor-based system" should be changed to --the processor-based system--.

Each of these changes has been made.

Section 102 Rejection

Starting in paragraph 4, the claims were rejected under Section 102. The objections are addressed to the extent possible. However, the failure to specifically address each claim hamstrings the applicant in adequately responding in detail to each of the objections raised. It is respectfully submitted that generalized or grouped rejections are not proper. See M.P.E.P. § 706.07 ("Before final rejection is in order, a clear issue should be developed between the Examiner and the applicant"); M.P.E.P. § 707(d) ("A plurality of claims should never be grouped together in a common rejection unless that rejection is equally applicable to all claims in the group").

Addressing the rejections that are made, it is respectfully submitted that nothing within any of the cited materials teaches adding two columns to the matrix for each circuit output that, as the same time, produces an unknown logic value. While Rajski mentions the problem of unknown logic values, his solution, as well as can be determined, is simply to mask them. See column 5, lines 47-48. He does not add two columns to a matrix to overcome the problem.

The same analysis applies to claim 9.

Claim 16 has been amended to call for doing what is claimed "without masking unknown logic values." The term has been added to claim 16 to clarify the claim and to distinguish on the same basis as described above.

Therefore, reconsideration is respectfully requested.

Respectfully submitted,

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